

Accelerating Computational Lithography: Enabling our Electronic Future Vivek Singh

VP, Advanced Technology Group, NVIDIA





Outline

- What is Computational Lithography?
- The Problem: Exploding Computation
- The Breakthrough!
- Enables Better Chip Technology, Faster
- Summary, and a quiz!





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Camera shopping tip: Buy largest aperture

- Aperture shown as ratio
- Need low denominator
- 2.0 is good, 1.4 excellent, and expensive

Aperture also appears in Rayleigh Criterion in diffractive optics



Warm up with photography

aperture







Federer, Indian Wells 2015



Low depth of field: good for pictures, bad for IC yield

Aperture in daily life



Large aperture (f/2.0) Low depth of field





Small aperture (f/7.1) High depth of field











NVIDIA Ampere











An Ant

Source: <u>serious-science.org</u>

https://serious-science.org/fire-ants-conquer-the-world-on-the-first-global-trade-network-2570







100 µm

EHT = 10.00 kV WD = 11.0 mm I Probe = 200 pA Signal A = SE1

Date :4 Jun 2009 Mag = 156 X Reference Mag = Polaroid 545

Grain of salt



Source: <u>Wikipedia</u>

https://en.wikipedia.org/wiki/Salt#/media/File:Single_grain_of_table_salt_(electron_micrograph).jpg





Human hair



Source: <u>nisenet.org</u>

https://www.nisenet.org/catalog/scientific-image-sem-image-human-hair







Red Blood Cell

Source: <u>Guardian</u>

https://www.theguardian.com/science/2022/nov/07/new-hope-for-sickle-cell-patientsas-uk-trial-of-lab-grown-red-blood-cells-begins







Spot Magn Det WD Exp 50000x SE 8.9 17 CACO cellen prer 10.0 kV 1.0 50000x SE

E. Coli Bacteria



Source: The Universe of E. Coli

https://www.intechopen.com/chapters/68841







Coronavirus

Source: <u>CDC</u>

https://www.cdc.gov/dotw/covid-19/index.html









5nm Transistor

Source: Bhoir, et al (2019). IEEE J. Electron Devices Society. http://dx.doi.org/10.1109/JEDS.2019.2934575





Too small for the light we use... ...have to find ways to bridge the gap

Source: <u>Wikipedia</u> https://en.wikipedia.org/wiki/Moore%27s_law





Wafer

Lithography stepper, simplified



When feature is small, image is blurred





Wafer

Can we "bend" light by inverting the problem?



Given an image, what mask and source do I need?

Wafer

Answer: Computational Lithography Input = design, output = mask + source

$$\begin{aligned}
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& \int \int E \cdot dS &= \frac{1}{\varepsilon_0} \iiint \rho \, dV \\
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\end{aligned}$$

Computational Lithography

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Summary, and a quiz!

Increasing need for mask correction

- From simple decorations to complex "distortions"
- Intuition finally breaks down

NVIDIA,

Billions of transistors on a chip

25		
Z .J		
2.0 -		
1.5 -		
1.0 -		
0.5 -		
0.0 -		

... trillions of polygons on a chip

NVIDIA chips

	_ 13000	
	12000 -	
produc d by TSMC)	11000 -	
ber of nufactured	10000 -	
	9000 -	
	8000 -	2013

Sources: https://investor.tsmc.com/english/annual-reports_ https://www.statista.com/statistics/1178174/taiwan-semiconductor-manufacturing-company-number-of-products/

... and thousands of chips

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Can't just keep adding datacenters

Process node, nm

Sources: S. Jones (2020), Nikon Lithovision

V. Singh (2022). SPIE Advanced Lithography Conference Keynote

ILT Performance Is Getting Faster GPUs are reducing ILT simulation times > 10x

Unleash Innovation

Test Conditions

Run on single Tesla V100

 Forward sim 1x has one-time warmup overhead

 Forward sim 20x used to mimic OPC and amortize warmup time

Note: Real OPC also includes geometric processing beyond simulation; can itself be expensive

Can GPU libraries be used for polygon ops?

Source: Courtesy of K. Ho of TSMC, GTC 2020

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First Digital Picture Tom Kilburn, University of Manchester, UK 1947

cuLITHO: accelerates computational lithography

CUDA, OptiX, cuFFT, cuBLAS, cuSolver, NPP, RAPIDS, NVComp, Thrust+CUB, ...

Search and visibility

Edge visibility

Polygon Booleans

Component Speedup

End-to-End OPC Speedup Mask processing overnight, instead of 2 weeks

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Chip Design

Inverse Mask

Standard OPC

Curvilinear ILT

ILT Curvilinear Mask Delivers Superior Process Window

Curvilinear ILT vs. Standard OPC

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How broadly is inverse lithography (ILT) used for production chips today (2022)? (use includes for hot spots only; ILT refers to both Manhattanized ILT & Curvilinear ILT)

eBeam Initiative luminaries survey results, 2022. https://www.ebeam.org/docs/2022-ebeam-luminaries-survey-final-1.pdf

> 90%

IVIDIA

If OPC, ILT are 40X faster...

- How much does that speed up
 - Each experiment in the Fab?
 - Each product stepping?
 - A technology node's time-to-yield?
 - A product's time-to-market?

"The culitho team has made admirable progress on speeding up computational lithography by moving expensive operations to GPU. This development opens up new possibilities for TSMC to deploy lithography solutions like Inverse Lithography Technology (ILT) and Deep-Learning more broadly in chip manufacturing, making important contributions to the continuation of semiconductor scaling"

Partnership with TSMC

- Dr. C.C. Wei, CEO, TSMC

Partnership with ASML

"We are planning to integrate support for GPUs into all of our computational lithography software products. Our collaboration with NVIDIA on GPUs and culitho should result in tremendous benefit to computational lithography, and therefore to semiconductor scaling. This will be especially true in the era of High NA EUV Lithography."

– Peter Wennink, CEO, ASML

Partnership with Synopsys

"Computation lithography, specifically Optical Proximity Correction (OPC) is pushing the boundaries of compute workloads for the most advanced chips. By collaborating with our partner, NVIDIA, to run Synopsys OPC software on the CULitho Platform, we massively accelerated the performance from weeks to days! The team-up of our two leading companies continues to force amazing advances in the industry."

Aart de Geus, Chair and CEO, Synopsys

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"The semiconductor industry is essential in driving every other industry in the world and advancing its capabilities is key to the future of innovation. As current technology nears the limits of physics, NVIDIA's introduction of culitho is helping to unlock this potential. Working with our partners TSMC, ASML and Synopsys, we can increase their throughput, decrease cycle time and accelerate speed to market, opening the door to innovations in a wide range of fields."

– Jensen Huang, Founder and CEO, NVIDIA

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How will this mask print?

